What is claimed is:

1. A semiconductor device wherein the direct current consumption circuit includes a reference voltage generation circuit that generates a reference voltage from a power supply voltage, and the macro circuit includes:

a first switching circuit connected to the reference voltage generation circuit for cutting off the direct current that flows in the reference voltage generation circuit in response to the stop signal;

a start signal generation circuit for generating a start signal when the stop signal is deactivated; and

a second switching circuit connected to the reference voltage generation circuit and the start signal generation circuit for starting the reference voltage generation circuit in response to the start signal.

2. The semiconductor device of claim 1, wherein the macro circuit includes:

a data transfer circuit for generating a transfer data signal from an input data signal in accordance with a clock signal;

a first reset circuit connected to the data transfer circuit for resetting the transfer data signal of the data transfer circuit in response to a reset signal;

a power-on reset circuit connected to the first reset circuit for generating the reset signal when power is provided thereto;

a start signal generation circuit for generating a start signal when the stop signal is deactivated; and

a second reset circuit connected to the start signal generation circuit and the data transfer circuit for resetting the transfer data signal in response to the start signal.

3. The semiconductor device of claim 1, wherein the macro circuit includes:

a data transfer circuit for generating a transfer data signal from an input signal in accordance with a clock signal;

a power-on reset circuit for generating a reset signal when power is provided thereto;

a start signal generation circuit for generating a start signal when the stop signal is deactivated;

a composite circuit connected to the power-on reset circuit and the start signal generation circuit for generating a composite reset signal by combining the start signal and the reset signal; and

a reset circuit connected to the composite circuit for resetting the transfer data signal in response to the composite reset signal.

4. The semiconductor device of claim 1, wherein the macro circuit includes:

a data transfer circuit for generating a transfer data signal from an input data signal in accordance with a clock signal;

a power-on reset circuit for generating a reset signal when power is provided thereto;

a composite circuit connected to the power-on reset circuit for generating a composite reset signal by combining the stop signal and the reset signal; and

a reset circuit connected to the composite circuit for resetting the transfer data signal in response to the composite reset signal.

5. The semiconductor device of claim 1, further comprising:

a first external terminal connected to the direct current consumption circuit for receiving the stop signal; and

a second external terminal connected to the logic circuit, wherein the second external terminal is used to supply a test signal for performing a current test of the logic circuit.